REMARKS

Claims 43, 52, 54, 56, 109-110,113-118,126-128 of the subject application are currently pending, and have been rejected by the Examiner. In the accompanying amendment, claims 50, 111-112, and 119-125 have been cancelled, and claims 43, 52, 54, 56,109-110,113-114,116,118, and 126-128 have been amended. Further new claims 129-187 have been added. Support for the new claims can be found in the written description, claims, and drawings of the specification as originally filed. On account of the foregoing listed support for the new claims, it is respectfully submitted that the new claims do not add new matter.

DOUBLE PATENTING

In response to the provisional double patenting rejection of claims 43, 50, 52, 54, 56, and 109-128, the Applicant files herewith, a terminal disclaimer. In view of the terminal disclaimer, it is respectfully submitted that the Examiner should withdraw the provisional double patenting rejection.

CLAIMED REJECTIONS UNDER 35 USC § 112

Claims 50, 52, 54, and 126 stand rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention. As far as the 35 USC § 112, second paragraph rejection of claims 50 is concerned, this is now moot, as claim 50 has been cancelled.

Moreover, claims 52, 54, and 126 have been amended to accord with the provisions of 35 USC § 112, second paragraph. In view of these amendments, it is respectfully submitted the Examiner should withdraw the rejection of the claims 52,54, and 126 under 35 USC § 112, second paragraph.

CLAIM OBJECTIONS

The minor informalities in claim 126 as pointed out by the Examiner on page 5, paragraph 8 of the Office Action mailed June 6, 2005, have been corrected. The

Applicant thanks the Examiner for pointing out these informalities, and requests that the objections to claim 126 be withdrawn.

CLAIM REJECTIONS UNDER 35 USC § 102

The Examiner has rejected claims 43, and 122 under 35 USC § 102(e) as being anticipated by "Designing Hardware to Interpret Virtual Machine Instructions" by Otto Steinbusch (hereinafter "Steinbusch"), published February, 1998. The Applicants traverse.

Regarding claim 43, the Examiner states that:

> "The hardware accelerator marks variables associated with stack-based instructions in the register file as modified when the variables are updated as a result of the processing of the stack-based instructions to enable selective writing of the variables as marked as modified to memory (page 18, lines 13-18), where VMI generates MIPS instructions that cause to update (sic) registers in the VMI, indicates that VMI can modify the registers by selective writing. On paged (sic) 32, 36 show that different kinds of registers and the registers hold variables, paged 37, fourth paragraph shows the registers are labeled (marked) indicates that the variables can be marked".

(Office Action mailed June 6, 2005, pages 7 and 8.)

The Applicant respectfully disagrees with the Examiner's argument. In particular, by the Examiner's argument, the VMI of Steinbusch is the hardware accelerator and the pertinent portion of Steinbusch (page 18, lines 13-18) indicates that the CPU writes to the results to one of the VMI's registers. Thus, in accordance with the description in Steinbusch, it is the CPU that is writing to the VMI's registers, whereas the claimed limitation of claim 43 requires the hardware accelerator to mark variables as modified. The Examiner has thus failed to show that the hardware accelerator/VMI of Steinbusch marks variables as modified.

Moreover, the Examiner has simplistically equated the action of the CPU writing results to one of the VMI's registers to the action of the CPU marking the registers as modified. These two actions are not the same and, therefore, should not be equated. In this regard, the Examiner is respectfully request to consider that it is possible for the CPU to write to a register, without having to mark that register as having been modified. Further, the CPU writing results to one of the VMI registers, as described in Steinbusch, does not indicate that such writing can be or is selective. Thus, it is respectfully submitted that Steinbusch page 18, lines 13-18 does not support the Examiner's argument that Steinbusch teaches "a hardware accelerator to process stack-based instructions in cooperation with the CPU core, wherein the hardware accelerator marks variables associated with the stack-based instructions in the register file as modified when the variables are updated as a result of the processing of the stack-based instructions to enable selective writing of the variables marked as modified to a memory", as recited in claim 43.

Steinbusch page 37, fourth paragraph merely describes that the output of a MIPS instruction is placed on the output labeled "i2FIFO". It is important to appreciate that the system of Steinbusch is not doing any marking or labeling, as suggested by the Examiner, but rather sending or placing an instruction on the output labeled as "i2FIFO". That this interpretation is proper becomes more evident when the quoted portion of Steinbusch is rewritten as "this instruction is placed on the output indicated as "i2FIFO".

In the light of the foregoing, the Examiner is respectfully requested to reconsider her arguments. The Applicants repeat that Steinbusch does not teach or suggest the limitation of "the hardware accelerator marking variables associated with the stack-based instructions in the register file as modified when the variables are updated as a result of the processing of the stack-based instructions to enable selective writing of the variables marked as modified to a memory" , as recited in claim 53.

Based on the foregoing, it is respectfully submitted that Steinbusch does not anticipate claim 43.

Regarding the rejection of claim 122 under 35 USC § 102, it is respectfully submitted that this rejection be withdrawn, as claim 122 has been cancelled.

Likewise, claim 124, and 125 have been cancelled, and the Examiner is respectfully requested to withdraw her rejection of these claims.

CLAIM REJECTIONS UNDER 35 USC § 103

Claims 50, 52, 54, 56, 109-121, and 126-128 stand rejected under 35 USC § 103(a) as being unpatentable over Steinbusch and further in view of Tremblay (US6,125,439). Applicants traverse.

Claim 50 has been cancelled. Therefore, the Examiner is respectfully requested to withdraw her rejection of this claim.

Regarding claim 52, this claim includes the limitation "*wherein the hardware accelerator generates a new virtual machine program counter (PC) due to a "JSR" or "JSR_W" bytecode by sign extending an immediate branch offset following the "JSR" or "JSR_W" bytecode*' (emphasis added). With regard to this limitation the Examiner merely states that Steinbusch discloses conditional and unconditional jumps. Applicants respectfully submit that when the Examiner considers the entire limitation of claim 52 quoted above, the Examiner will realize that neither Steinbusch nor Tremblay, either individually or in combination teach or suggests the above-quoted limitation of claim 52. Accordingly, it is respectfully submitted that claim 52 and its dependent claims are not anticipated or rendered obvious by the combination of Steinbusch and Tremblay proposed by the Examiner. Moreover, the Applicants contend that the Examiner has failed to make a prima facie case of obviousness because the Examiner has failed to show why one of ordinary skill in the art would be motivated to combine the teachings of Tremblay and Steinbusch. In this regard, it is not seen how the Examiner's statement that "one of ordinary skill in the art would be motivated to implement the system to write back the value into the register" relates to the limitations of claim 52.

Regarding claim 54, this claim includes the limitation "*wherein the hardware accelerator performs sign extension for virtual machine SiPush and BiPush bytecodes and appends the sign extended data to an immediate field of a register-based instruction being composed based on the stack-based instructions*" (emphasis added). Based on the Examiner's argument regarding the rejection of claim 54, it appears that the Examiner has focused only on selected words from the above-quoted limitation of claim 54. For example, focusing on "SiPush" and "Bipush" the Examiner refers to col 43 lines 8-20 of the Tremblay reference. Again, focusing on "sign extension" the Examiner refers to col 65 lines 54-55 of the Tremblay reference. However, the Examiner does not show where Tremblay or Steinbush teaches or suggests the entire limitation of claim 54 as quoted above. In this regard, is respectfully submitted that the combination of Tremblay and Steinbusch suggested by the Examiner fails to teach or suggest the above-quoted limitation of claim 54. At any event, the Applicants contend that the Examiner has failed to make a prima facie case of obviousness because the Examiner has failed to show why one of ordinary skill in the art would be motivated to combine the teachings of Tremblay and Steinbusch. In this regard, the Examiner's statement that "one of the ordinary skill in the art would be motivated to insert the new items into the stack" (sic) does not bear scrutiny as it does not show why that should be so. Accordingly, it is respectfully submitted that claim 54 and its dependent claims are not anticipated or rendered obvious by the combination of Steinbusch and Tremblay proposed by the Examiner.

Regarding claim 119-121, these claims have been cancelled. Accordingly, the Examiner is respectfully requested to withdraw the rejection of these claims.

Regarding claim 56, this claim includes the limitation "*wherein the hardware accelerator performs sign extension for virtual machine SiPush and BiPush bytecodes and makes the sign extended data available to be read by the execute logic*". The above arguments made in connection with the rejection of claim 54 are repeated with respect to the above-quoted limitation of claim 56. Accordingly, it is respectfully submitted that claim 56 and its dependent claims are not anticipated or rendered obvious by the combination of Steinbusch and Tremblay proposed by the Examiner.

Regarding claims 109-118, these claims depend on claim 43, and, thus, include all limitations of claim 43. Accordingly, based on the arguments in connection with the rejection under 35 USC § 102, presented above, it is respectfully submitted that these claims cannot be rendered obvious in view of the Steinbusch/Tremblay combination, as the Steinbusch/Tremblay combination fails to teach or suggest the "marking variables limitation" of claim 43, discussed above.

For the reasons stated above claims 126-128, are also not rendered obvious in view of the combination of Steinbusch and Tremblay.

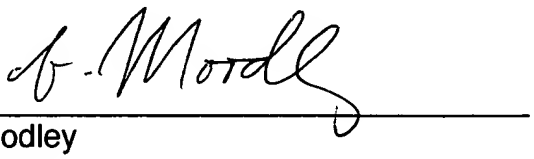
Applicant respectfully submits that the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Vani Moodley at (650) 903-2257.

Please charge any shortages and credit any overages to Deposit Account No. 503437. Any necessary extension of time for response not already requested is hereby requested. Please charge any corresponding fee to Deposit Account No. 503437.

Respectfully submitted,

HAHN & MOODLEY LLP

Date: 12/1/2005



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